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10/699,909	11/03/2003	Jason Harold Culler	200310794-1	5350

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EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,909	CULLER, JASON HAROLD	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18 and 20-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-16,18,20-22 and 24-37* is/are rejected.

7)☒ Claim(s) *10 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 6/9/06.

2. Claims 1-5, 7, 9-12, 15-16, 18, 20-25, 29-30 have been amended and claims 17, 19 have been cancelled. Thus, claims 1-16, 18, 20-37 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 5-6, 9, 11, 14, 25-32, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sander (US Patent Application No 2002/0168043), in view of Sander (US Patent 6269135)

For claim 1, Sander (US Patent Ap0plication No 2002/0168043) teaches the following limitations:

A system comprising:

a sample network (Fig 4 and Fig 5) **that provides plural samples of an input signal state associated with different time instances of the input signal** (lines 1-3 of [0032] of page 2 Q1 and Q2 produces a divide by 4 version of Fx. Output from Q3 is the divide by 4 of Fx, which is the input signal)

a detector that provides an indication of a frequency for the input signal (sum value provides the indication of frequency for Fx. Output of Q3, the input signal to the chain, is divide-by-4 of Fx. Therefore, indication of Fx implies indication of the input signal) **on samples of the input signal state for different time instances of the input signal residing within one period of the input signal** (Fig 5 shows the output from Q10 at the top of Q10. The output of Q10 is based on one clock cycle of the input signal), **the detector provides a value that represents the frequency of the input signal** (The detector produces "Sum" signal, which provides indication of frequency for the input signal based on the plural indications of signal state. A "0" value of Sum indicates Fx<Fs. A "2" value indicates Fx>Fs).

Sander (US Patent Application No 2002/0168043) does not teach that the detector determines the frequency of the input signal.

Sander (US Patent 6269135) teaches a system where a detector (filter described by Fig 8) determines the frequency of the input signal (Fx is determined as normalized over Fs. Thus, the filter of Fig 8 determines Fx in terms of Fs) based on samples of input signal state for different time instances (Fig 8 shows that ratio of Fx/Fs can be obtained for 1 samples), the detector provides a value that represents the determined frequency (the output of filter is the ratio that represents the frequency).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Sander (US Patent Ap0plication No 2002/0168043) and Sander (US Patent 6269135). Since, Sander (US Patent Ap0plication No 2002/0168043) is an extension of Sander (US Patent 6269135), one ordinary skill in the art would be motivated to employ the teachings of Sander (US Patent 6269135) into Sander (US Patent Ap0plication No 2002/0168043) to determine the frequency of unknown signal and derived signal. Such detectors can ensure high accuracy (lines 48-49 of column 4).

For claims 2, 9 and 11, 405es are the plurality of storage elements arranged to provide output samples of Sum.

For claim 5, clock signal activates the storage elements in Fig 5. However, Sander does not teach that the oscillator generates the clock signal.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 6, Fs can be higher or lower than the frequency of input signal.

For claim 14, Sander does not teach that the system is within an integrated circuit chip.

Examiner takes an official notice that the system implemented within the IC chip is well known in the art. An ordinary skill in the art would have been motivated to implement the system within the IC chip for many reasons, such as, to make commercially available to the customers.

For claims 25 and 30, Sander (US Patent Ap0plication No 2002/0168043) teaches the following limitations:

A frequency detection system comprising:

means for sampling an input signal having an unknown frequency and for providing plural indications of signal state associated with different time instances of an input signal (lines 1-3 of [0032] of page 2 Q1 and Q2 produces a divide by 4 version of Fx. Output from Q3 is the divide by 4 of Fx, which is the input signal); **and**

means for determining indication of a frequency for the input signal based on the plural indications of signal state (sum value provides the indication of frequency for Fx. Output of Q3, the input signal to the chain, is divide-by-4 of Fx. Therefore, indication of Fx implies indication of the input signal) **that correspond to time instances of the input signal based on plural indications of signal state that correspond to time instances of the input signal residing within a single period of**

the input signal (Fig 5 shows the output from Q10 at the top of Q10. The output of Q10 is based on one clock cycle of the input signal); **and**

means for providing a corresponding indication of frequency value for the determined frequency (The detector produces "Sum" signal, which provides indication of frequency for the input signal based on the plural indications of signal state. A "0" value of Sum indicates Fx<Fs. A "2" value indicates Fx>Fs)..

Sander (US Patent Ap0plication No 2002/0168043) does not teach that the detector determines the frequency of the input signal.

Sander (US Patent 6269135) teaches a system where a detector (filter described by Fig 8) determines the frequency of the input signal (Fx is determined as normalized over Fs. Thus, the filter of Fig 8 determines Fx in terms of Fs) based on samples of input signal state for different time instances (Fig 8 shows that ratio of Fx/Fs can be obtained for 1 samples), the detector provides a value that represents the determined frequency (the output of filter is the ratio that represents the frequency).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Sander (US Patent Ap0plication No 2002/0168043) and Sander (US Patent 6269135). Since, Sander (US Patent Ap0plication No 2002/0168043) is an extension of Sander (US Patent 6269135), one ordinary skill in the art would be motivated to employ the teachings of Sander (US Patent 6269135) into

Sander (US Patent Ap0plication No 2002/0168043) to determine the frequency of unknown signal and derived signal. Such detectors can ensure high accuracy (lines 48-49 of column 4).

For claims 26 and 27, Q3-Q6 delays the input signal, which is a clock signal.
For claim 28, Q7, Q11, Q15 and Q19 are storing signal states.

For claim 29, Fig 5 shows the comparison of Sum with Alias. Alias value is an indication of the expected frequency range of the unknown clock signal (abstract). Lines 8-11 of [0034] of page 2 mention that the number stream may be formed accordingly. Thus, the number stream follows the comparison of alias with sum. Therefore, a controller must be present to implement the adjustment of input clock signal based on comparison of sum with alias.

For claim 31, the storage elements Q7-Q19 of Fig 5 are activated by Fs and delayed Fx.

For claim 32, Fs is a clock signal that activates the storage elements.

For claim 34, Q3-Q6 are the delay elements that delay the propagation of the signal through the plurality of storage elements to establish the spaced apart time intervals.

For claim 35, Fs/Fx both are the clock signal that controls the activation of storage elements.

4. Claims 3-4, 7-8, 12, 15-16, 18, 20-22, 24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sander (US patent Application publication 2002/0168043), in view of Sanders (US Patent 6269135), further in view of Lee et al (US Patent 6326826).

For claims 3 and 4, Q3-Q6 of Fig 5 Sander (US patent Application publication 2002/0168043) are delay elements to provide respective delayed signals of input signal (lines 1-5 of [0029] and lines 1-5 of [0032] of page 2). The respective delayed input signals from Q3-Q6 activate the storage Q7, Q11, Q15, Q19 to provide the signal states of Fx to sample Fx at different time intervals.

However, combination of Sander and Sander does not teach delay elements providing respective delayed clock signals to clock the storage.

Lee et al teach the delay elements providing respective delayed clock to clock the substantial number of storage elements (Fig 1 and Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Sander, Sander and Lee et al. One ordinary skill in the art would be

motivated to use the DLL of Lee et al into the combination system of Sander and Sander, since the DLL of Lee et al can work over a wide variety of ranges and provide protection against false locking (lines 56-59 of column 1).

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For claim 7, Q3-Q6 of Fig 5 Sander (US patent Application publication 2002/0168043) are delay elements to provide respective delayed signals of input signal (lines 1-5 of [0029] and lines 1-5 of [0032] of page 2). The respective delayed input signals from Q3-Q6 activate the storage Q7, Q11, Q15, Q19 to provide the signal states of Fx to sample Fx at different time intervals.

However, combination of Sander and Sander does not teach delay elements providing respective delayed clock signals to clock the storage. Lee et al teach a system where delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 8, the delay elements in 11 of Lee et al are connected in series.

For claim 12, Fig 5 shows the comparison of Sum with Alias. Alias value is an indication of the expected frequency range of the unknown clock signal (abstract). Lines 8-11 of [0034] of page 2 mention that the number stream may be formed accordingly. Thus, the number stream follows the comparison of alias with sum. Although combination of

Sander and Sander does not teach a controller to adjust the clock signal, the system of Lee adjusts the clock signal. One ordinary skill in the art would be motivated to use the DLL of Lee et al into the combination system of Sander and Sander, since the DLL of Lee et al can work over a wide variety of ranges and provide protection against false locking (lines 56-59 of column 1).

For claim 15, Q7, Q11, Q15 and Q19 of Fig 5 of Sander (2002/0168043) are the plurality of storage elements being activated to latch different time instances of an input signal to provide corresponding output samples (output from Q10, Q14, Q18 and Q22) sufficient for determining frequency characteristics of the input signal ("Sum" provides indication of frequency. Note [0029]; [0030]). However, Sander does not determine the frequency nor delay elements provide respective clock signal.

Sander (US Patent Ap0plication No 2002/0168043) does not teach that the detector determines the frequency of the input signal.

Sander (US Patent 6269135) teaches a system where a detector (filter described by Fig 8) determines the frequency of the input signal (Fx is determined as normalized over Fs. Thus, the filter of Fig 8 determines Fx in terms of Fs) based on samples of input signal state for different time instances (Fig 8 shows that ratio of Fx/Fs can be obtained for 1 samples), the detector provides a value that represents the determined frequency (the output of filter is the ratio that represents the frequency).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Sander (US Patent Ap0plication No 2002/0168043) and Sander (US Patent 6269135). Since, Sander (US Patent Ap0plication No 2002/0168043) is an extension of Sander (US Patent 6269135), one ordinary skill in the art would be motivated to employ the teachings of Sander (US Patent 6269135) into Sander (US Patent Ap0plication No 2002/0168043) to determine the frequency of unknown signal and derived signal. Such detectors can ensure high accuracy (lines 48-49 of column 4).

However, combination of Sander and Sander does not teach delay elements providing respective delayed clock signals to clock the storage.

Lee et al teach the delay elements providing respective delayed clock to clock the substantial number of storage elements (Fig 1 and Fig 2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Sander, Sander and Lee et al. One ordinary skill in the art would be motivated to use the DLL of Lee et al into the combination system of Sander and Sander, since the DLL of Lee et al can work over a wide variety of ranges and provide protection against false locking (lines 56-59 of column 1).

For claim 16, Sum block and Decision logic block of Fig 5 can be treated as a detector, since they provide indication of frequency. Fig 5 shows the output from Q10 at the top of Q10. The output of Q10 is based on one clock cycle of the input signal, i.e., output of Q3.

For claim 18, input signal is delayed by Q3-Q6 to provide delayed signals for activating the substantial number of storage elements.

For claim 20, clock signal activates the storage elements in Fig 5. However, Sander does not teach that the oscillator generates the clock signal.

Examiner takes an official notice that the oscillator generating clock signal is well known in the art. An ordinary skill in the art would have been motivated to have an oscillator providing the clock signal, since oscillator provides an on-chip generation of clock signal.

For claim 21, Lee et al teach that the delay elements (18') provide respective clock edges (CK[1:7] in Fig 2) for activating the storage elements (22'), each of the clock edges corresponding to a different delayed version of the clock signal (11).

For claim 22, the delay elements in 11 of Lee et al are connected in series.

For claim 24, Q7, Q11, Q15 and Q19 of Sander are the plurality of storage elements that are activated to latch output samples to the detector "Sum" box to provide the output samples (output of Q10, Q14, Q18,Q22) that represent different time instances of signal state for the input signal.

For claim 33, Fig 1 of Lee et al shows the delaying of a clock signal to provide the clock edges.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Sander and Lee et al. One ordinary skill in the art would have been motivated to delay the clock signal to provide clock edges as shown in Lee et al, since the approach is popular in DLL based clock control. Such arrangement could be beneficial to the system of Sander to avoid the stability problem (lines 45-47 of column 1 in Lee et al).

5. Claim 13, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sander (US patent Application publication 2002/0168043), Sander (US Patent 6269135) in view of Elbe et al (US Patent Application Publication 2004/0139363).

For claims 13 and 36, combination of Sander and Sander does not teach that the oscillator generates the input signal as a clock signal having a frequency based on a controller output signal.

Elbe et al teach a system comprising an oscillator that generates the input signal as a clock signal having a frequency based on a controller output signal (170 is controlling 100a and 100b to produce f1 and f2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Sander and Elbe et al. One ordinary skill in the art would have been motivated to have a controllable oscillator controlled by a controller output to produce a variable frequency, since that would ensure the peripheral units to have a controllable frequency that can be increased on demand.

For claim 37, oscillator of Elbe et al can change the frequency.

Allowable Subject Matter

Claims 10 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed on 6/9/2006 are moot in view of new grounds of rejections. However, Sander and Lee are relied upon for rejection, examiner is addressing the relevant arguments.

Applicant argues that Lee provides variable delay in the delay elements – not the fixed delay.

Examiner disagrees. The delay of Lee et al can be adjusted but it is able to provide fixed known delay. Line 29 of column 4 mentions that delay chain has minimum delay time. The minimum delay is the delay when all delay elements have minimum delay. Therefore the system is able to provide known fixed delay.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

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